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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/866,092
Filing Date: May 23, 2001
Appellant(s): MCCORMACK ET AL.

Brian W. Oaks
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 2/18/08 appealing from the Office action mailed 11/26/07. An amended appeal brief that corrects deficiencies in the previous appeal brief was filed 4/4/08.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,154,366	MA	11-2000
5,866,952	WOJNAROWSKI	2-1999
6,861,284	HIGASHI	3-2005
5,565,706	MIURA	10-1996
5,739,188	DESAI	4-1998
5,241,456	MARCINKIEWICZ	8-1993
5,953,619	MIYAZAWA	9-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

DETAILED ACTION

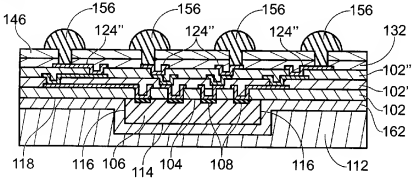
Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 17, 33, 34, 38, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. 6,154,366 in view of Wojnarowski et al. 5,866,952 in view of Higashi et al. 6,861,284 B2. Ma discloses (see, for example, Fig. 2j) a package (multi-layer printed circuit board) comprising an encapsulation material (circuit board substrate) 112 having a first substrate surface and a second substrate surface, die (first integrated electronic component) 106, cavity, flex component (first dielectric layer) 102, conductive trace (metallic layer) 124, electrically conductive first via, element (second dielectric layer) 102', and electrically conductive second via.

Fig. 2j



Ma does not disclose the circuit board substrate being polymeric. However, Wojnarowski discloses (see, for example, FIG. 1(e)) an integrated module substrate comprising a chip 14, and substrate molding material (circuit board substrate) 24. In column 7, lines 50-62, Wojnarowski discloses the substrate molding material being polymers (polymeric). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the circuit board substrate being polymeric in order to have a material that adequately supports a die in a substrate form, and any overlying layers wherein the material is not prone to cracking.

Ma in view of Wojnarowski does not disclose a second electrically conductive via extending at one location. However, Higashi discloses (see, for example, Fig. 7) a substrate 10 comprising a wiring pattern (second electrically conductive via) 18 in a via hole. The wiring traverses multiple insulating layers. It would have been obvious to one of ordinary skill in the art at the time of invention to have a second electrically conductive via extending at one location in order to lessen manufacture time, and save material.

Regarding claims 33, and 34, Ma discloses (see, for example, FIG. 1d) multiple conductive traces (at least one metal-lined via) 124. The multiple conductive traces transmit signals to the die.

Regarding claims 38, and 39, these claims contain product-by-process limitations (i.e. is fabricated at a temperature higher than the maximum processing temperature of the printed circuit board (claim 38), and at a temperature of greater than about 600 C (claim 39)) that do not structurally differentiate the applicant's claimed structure from Ma in view of Wojnarowski in view of Higashi.

3. Claims 18, 20 thru 23, 27, 30, 36, 40, 41, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. '366 in view of Wojnarowski et al. '952 in view of Higashi et al. '284 B2 as applied to claims 17, 33, 34, 38, and 39 and further in view of Miura et al. 5,565,706. Ma in view of Wojnarowski in view of Higashi does not disclose a first metallic layer disposed on said first substrate surface and a second metallic layer disposed on said second substrate surface. Miura discloses (see, for example, FIG. 6) a multi-layer package board (multi-layer printed circuit board) comprising a package board 46 having external output terminals (first metallic layer) 8 and external output terminals (second metallic layer) 28. It would have been obvious to one of ordinary skill in the art at the time of invention to have a first metallic layer disposed on said first substrate surface and a second metallic layer disposed on said second substrate surface in order to include external connections to the substrate such as voltages, metallizations, etc.

Regarding claims 20-23, see, for example, FIG. 6 wherein Miura discloses a via going through the package board 46 that connects the exteran louput terminals and other metal layers in the dielectric layers.

Regarding claim 27, see figures wherein Miura discloses external output terminals (conductive pad) 8 on top of the LSI 35.

Regarding claim 30, see FIG. 6 wherein Miura discloses one of the vias (at least one metal-lined via) 16 attached to LSI 33.

Regarding claim 36, see, for example, column 8, lines 25-28 wherein Miura discloses a capacitor.

4. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. '366 in view of Wojnarowski et al. '952 in view of Higashi et al. '284 B2 as applied to claims 17, 33, 34, 38, and 39 above, and further in view of Desai 5,739,188. Ma in view of Wojnarowski in view of Higashi does not disclose the multi-layer core substrate comprising at least two polymeric layers. However, Desai discloses (see, for example, column 3, lines 26-30) a multi layered product wherein the product comprises a substrate layer/cap layer (two polymeric layers). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the multi-layer core substrate comprising at least two polymeric layers in order to protect the substrate.

5. Claims 24, 26, 28, 29, 31, 32, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. '366 in view of Wojnarowski et al. '952 in view of Higashi et al. '284 B2 in view of Miura et al. '706 as applied to claims 18, 20-23, 27, 30, 36, 40, 41, and 43 above, and further in view of Marcinkiewicz et al. 5,241,456. Ma in view of Wojnarowski in view of Higashi in view of Miura does not disclose said exposed portion of said second substrate surface including a cavity additionally comprising a second integrated electronic component disposed in said cavity. However, Marcinkiewicz discloses (see, for example, FIG. 1) a structure 10 comprising a substrate 12, and chip (second integrated electronic component) 36. Having the chip in the same substrate creates a multichip device that saves space and provides interconnection between two chips. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have said exposed portion of said second substrate surface including a cavity additionally comprising a second integrated electronic component

disposed in said cavity in order to create a multichip device that saves space and provides interconnection between two chips.

Regarding claim 28, see, for example, FIG. 1 wherein Marcinkiewicz discloses contact pad (conductive pad) 38.

Regarding claim 29, see, for example, FIG. 1 wherein Miura discloses contact pad (conductive pad) 8 on top of the LSI 35.

Regarding claim 44, Miura in view of Wojnarowski in view of Higashi in view of Miura does not disclose a third dielectric layer disposed on said second side of said substrate. However, Marcinkiewicz discloses (see, for example, FIG. 1) a substrate 12, and dielectric layer (third dielectric layer) 52. The dielectric layer protects the bottom surface of the substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a third dielectric layer disposed on said second side of said substrate in order to protect the bottom of the substrate.

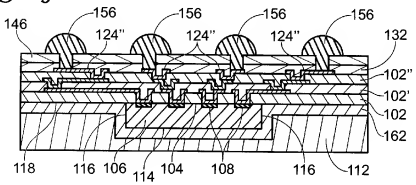
6. Claims 37, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable Ma et al. '366 in view of Wojnarowski et al. '952 in view of Higashi et al. '284 B2 in view of Miura et al. '706 as applied to claims 18, 20-23, 27, 30, 36, 40, 41, and 43 above, and further in view of Miyazawa et al. 5,953,619. Ma in view of Wojnarowski in view of Higashi in view of Miura does not disclose said capacitor comprising a perovskite capacitance material. However, Miyazawa discloses (see, for example, column 1, lines 27-35) that a perovskite crystal structure has a high dielectric constant. Therefore, it would have been obvious to one of ordinary skill in

the art at the time of invention to have said capacitor comprising a perovskite capacitance material in order to have a higher dielectric constant in the same area.

(10) Response to Argument

Regarding the appellant's argument on page 11 of the appeal brief filed 2/18/08 that the proposed combination of references does not disclose, teach or suggest a polymeric circuit board substrate having a cavity formed in a first substrate surface, this argument is not persuasive. In Fig. 2j, Ma clearly discloses a circuit board substrate 112 wherein its upper first surface contains a cavity wherein the cavity clearly contains a first integrated electronic component 106.

Fig. 2j



The appellant's argument that, in Ma, a component is surrounded, after having already been connected to a flex component, with an encapsulating materials and this technique is much different than securing a prefabricated component in a cavity that has been formed in a substrate, is not persuasive because the appellant's claims are directed towards product, and the method or the technique used are not patentable beyond what the final structure the method or technique entails which, in this case, is a substrate having a cavity formed in a first substrate surface. Ma

clearly discloses this final structural product as evidenced by Fig. 2j, and therefore, reads on the appellant's claimed structural limitations.

Regarding the appellant's argument on page 11, second paragraph that Applicants position is simply that there is no cavity disclosed in Ma, this argument is not persuasive. As already discussed before, the Examiner does not agree with the appellant's assessment that the board of Ma does not contain a cavity. It is bluntly and undeniably shown in Fig. 2j of Ma that there is a cavity in the circuit board substrate 112 as evidenced by the figure which shows a cavity containing the die in the middle of the circuit board substrate 112.

Regarding the appellant's argument on page 12 that Wojnarowski is brought in for the teaching of the substrate, this argument is not persuasive. Wojnarowksi is used to affirm that the circuit board substrate can be polymeric. Even though Ma does disclose the encapsulation material/substrate as plastic, it does not state that the plastic is polymeric. Even though it is understood that most plastics are polymeric, the Examiner wanted to remove all doubt that the circuit board substrate may be polymeric and decided to use Wojnarowski, which clearly discloses (see column 7, lines 50-62) that these kinds (i.e. substrates that carry chips) of substrates are known to be polymeric. In other words, Wojnarowksi is simply used to show that polymeric materials are one of many materials that may be used in a substrate to support a chip, and since Ma and Wojnarowski teach analogous structures (i.e. package comprising a chip on a substrate), it would been obvious to one of ordinary skill in the art to combine them in order to have a substrate that adequately supports a chip, and show, in Wojnarowski, that polymeric materials are one of those materials that serve this function. Regarding the appellant's argument near the bottom of paragraph two of page 12 that the flex component 102 of Ma is deemed to be

a substrate, this is not at all the case. The Examiner never deems in the final rejection or this examiner's answer that the flex component is the substrate.

Regarding the appellant's argument on page 13 that the Office Action has not provided a sufficient basis for combining the teachings of Ma with those of Wojnarowski, this argument is not persuasive. As already argued above, but further, the Examiner recognizes that references can not be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is NO requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971) references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA 1969). In this case, it would have been obvious to one of ordinary skill in the art to use polymers for the substrate in Ma in order to support a die, and any overlying layers, wherein the material is not prone to cracking. Wojnarowski shows this to be true as evidenced by Fig. 1(e) wherein a die 14 is formed in a cavity which is formed in a substrate 24.

The applicant's argument on page 14 regarding Miura is also not persuasive for the same reason (i.e. there is NO requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art). Miura discloses (see, for example, FIG. 6) a die 33 in a substrate 45 wherein the die is in a cavity. Miura shows that this same die can have additional connections wherein the connections are on a polymeric substrate. Such a

modification would be beneficial to Ma in view Wojnarowki in view of Higashi in order to connect dies to other dies and/or devices to make more intricate/robust devices (i.e. processors, etc). Therefore, Miura does provide the "articulated reasoning with some rational underpinning" as evidenced by FIG. 6.

Regarding the applicant's argument on page 15 that Desai teaches a wholly different art, this argument is not persuasive. It has been held that the determination that a reference is from a non-analogous art is two fold. First, we decide if the reference is within the field of the inventor's endeavor. If it is not, we proceed to determine whether the reference is reasonably pertinent to the particular problem with which the inventor was involved. In re Wood, 202 USPQ 171, 174. In this case, Desai teaches (see, for example, column 3, lines 28-31) how thermoplastic materials, which Ma in view of Wojnarowski in view of Higashi teaches in the polymeric board substrate, can be divided into two separate layers wherein one layer is the core and the other layer is protective. Applicant cites the cap layer may also hide imperfections of the core which would clearly be beneficial to the polymeric board substrate of Ma in view of Wojnarowski in view of Higashi. Since Ma in view of Wojnarowski in view of Higashi discloses polymeric substrates, and Desai also polymeric materials, it would have been obvious to one of ordinary skill in the art to combine Desai's teaching into Ma in view of Wojnarowski in view of Higashi in order to have a polymeric substrate with the same benefits.

The rest of the appellant's arguments are based on previous arguments which have already been addressed above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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